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100

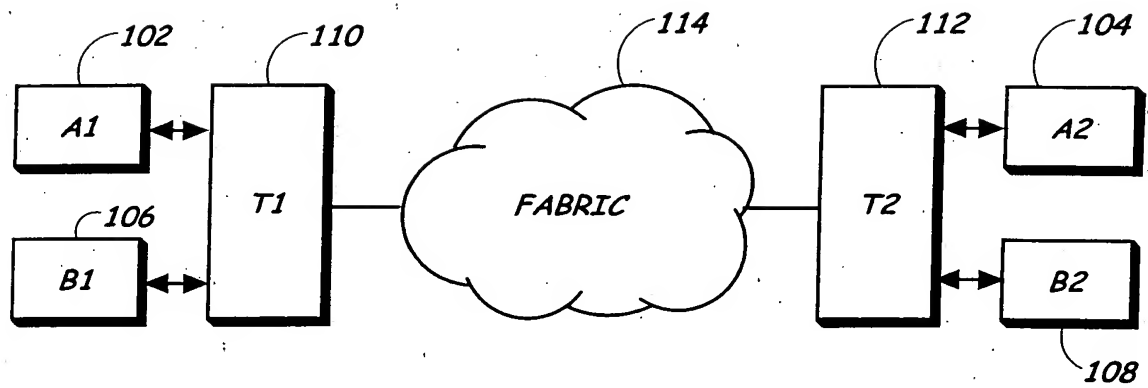


FIG. 1A

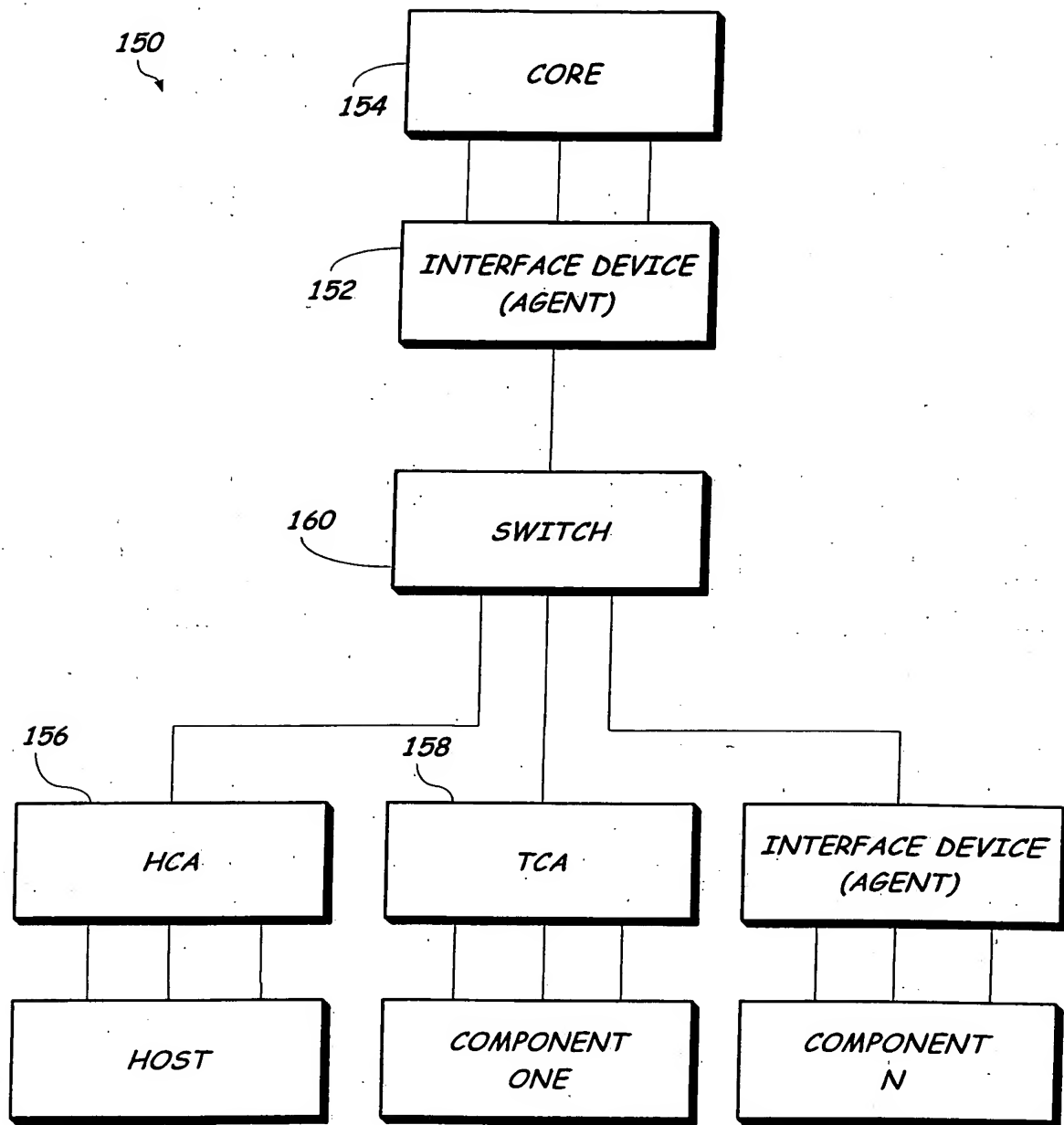
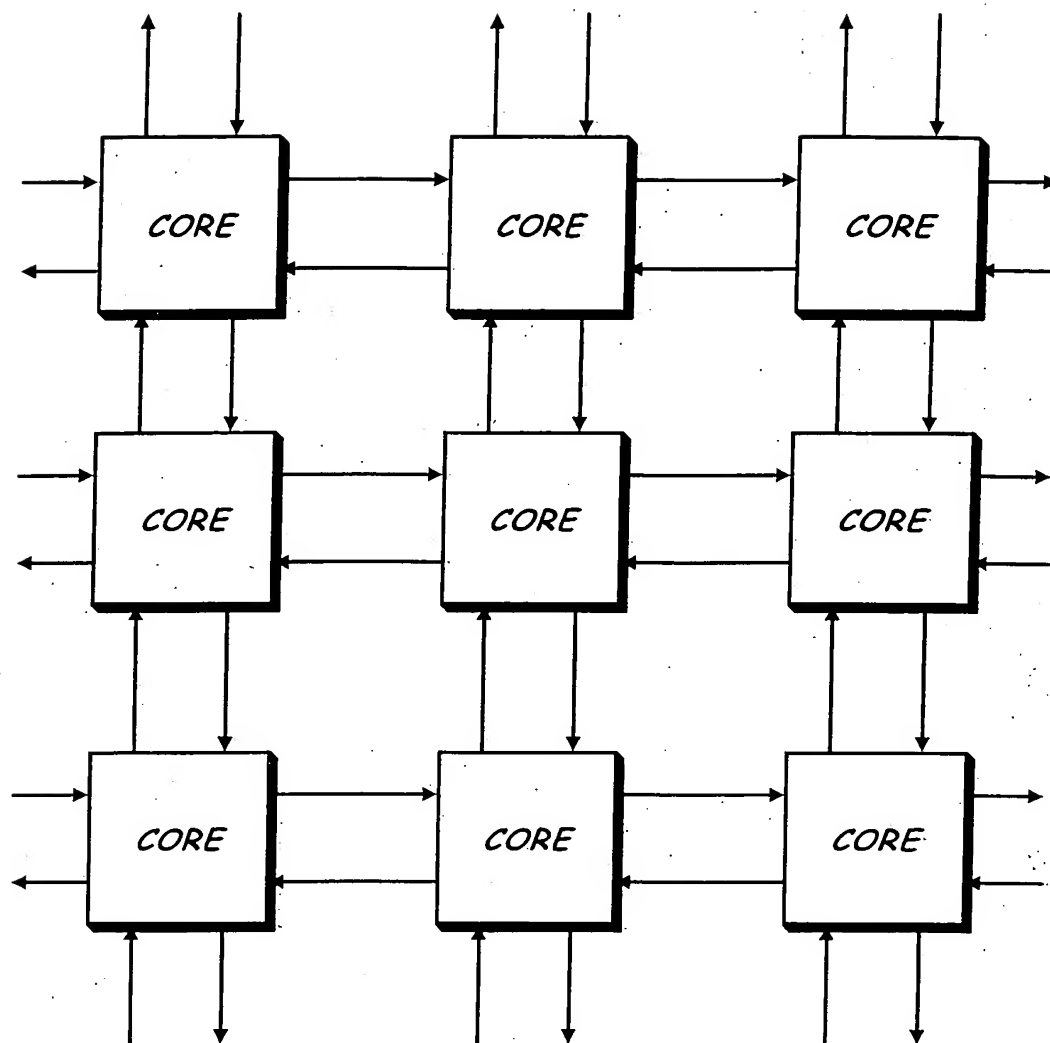


FIG. 1B

*FIG. 1C*

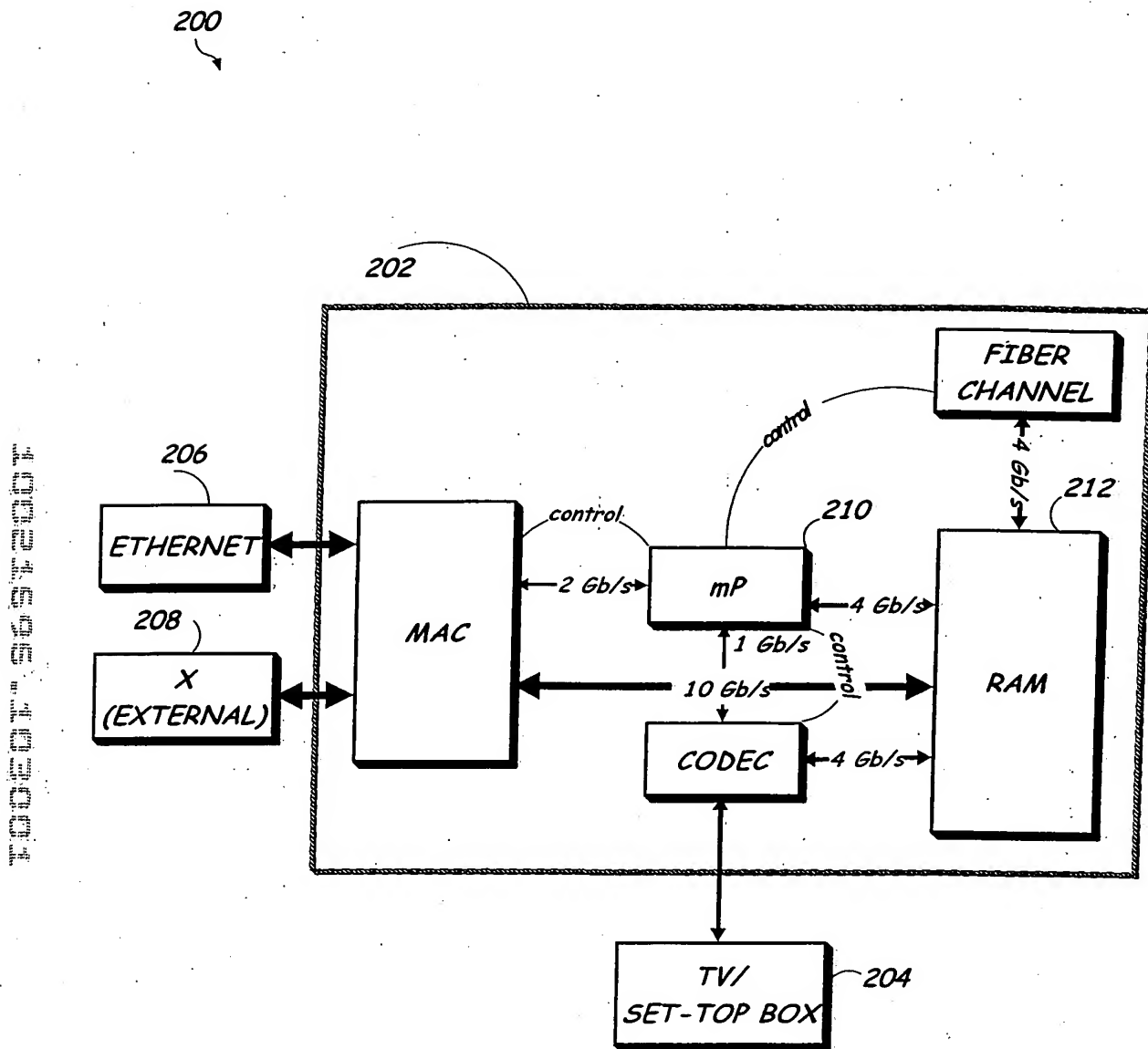
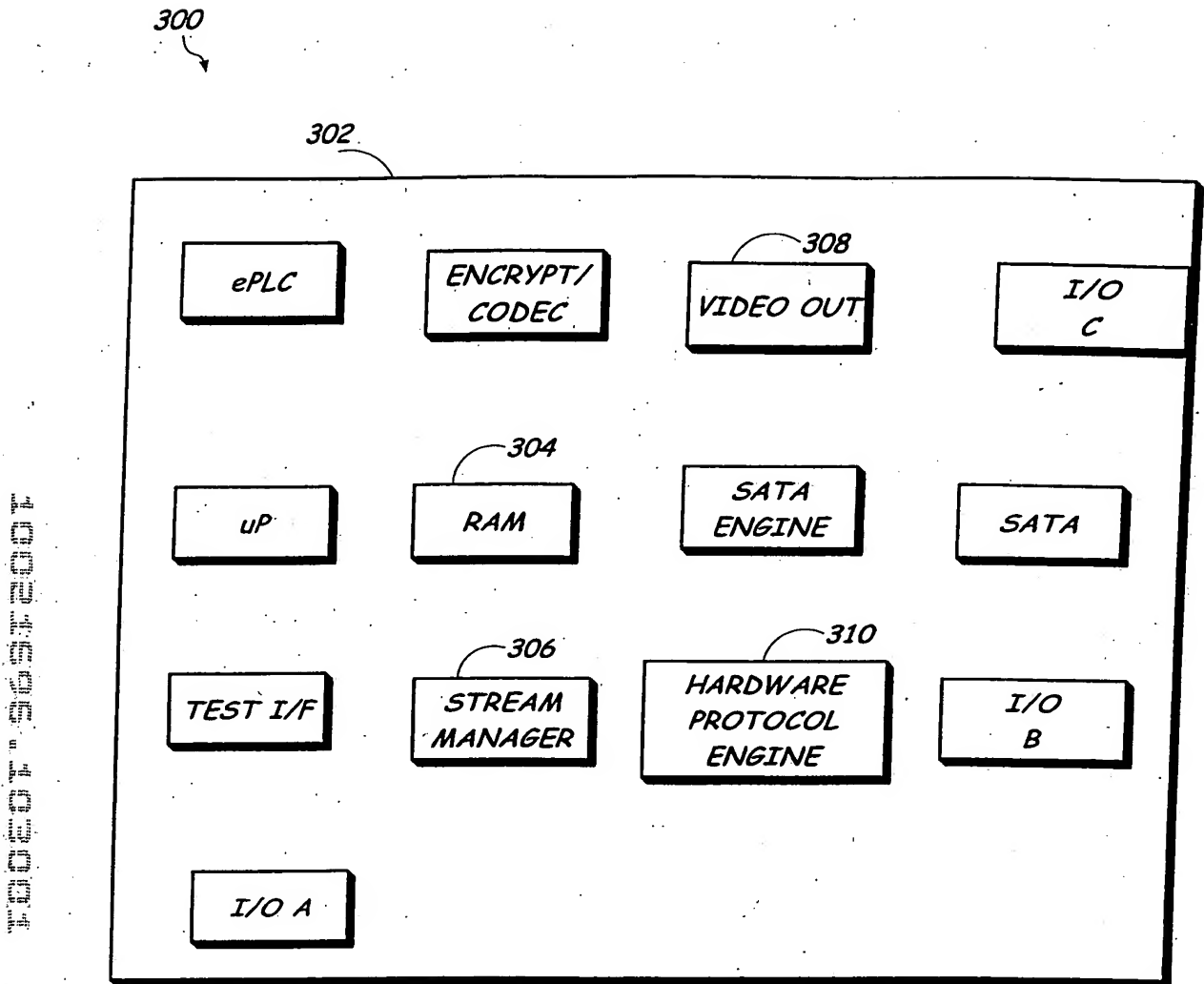


FIG. 2



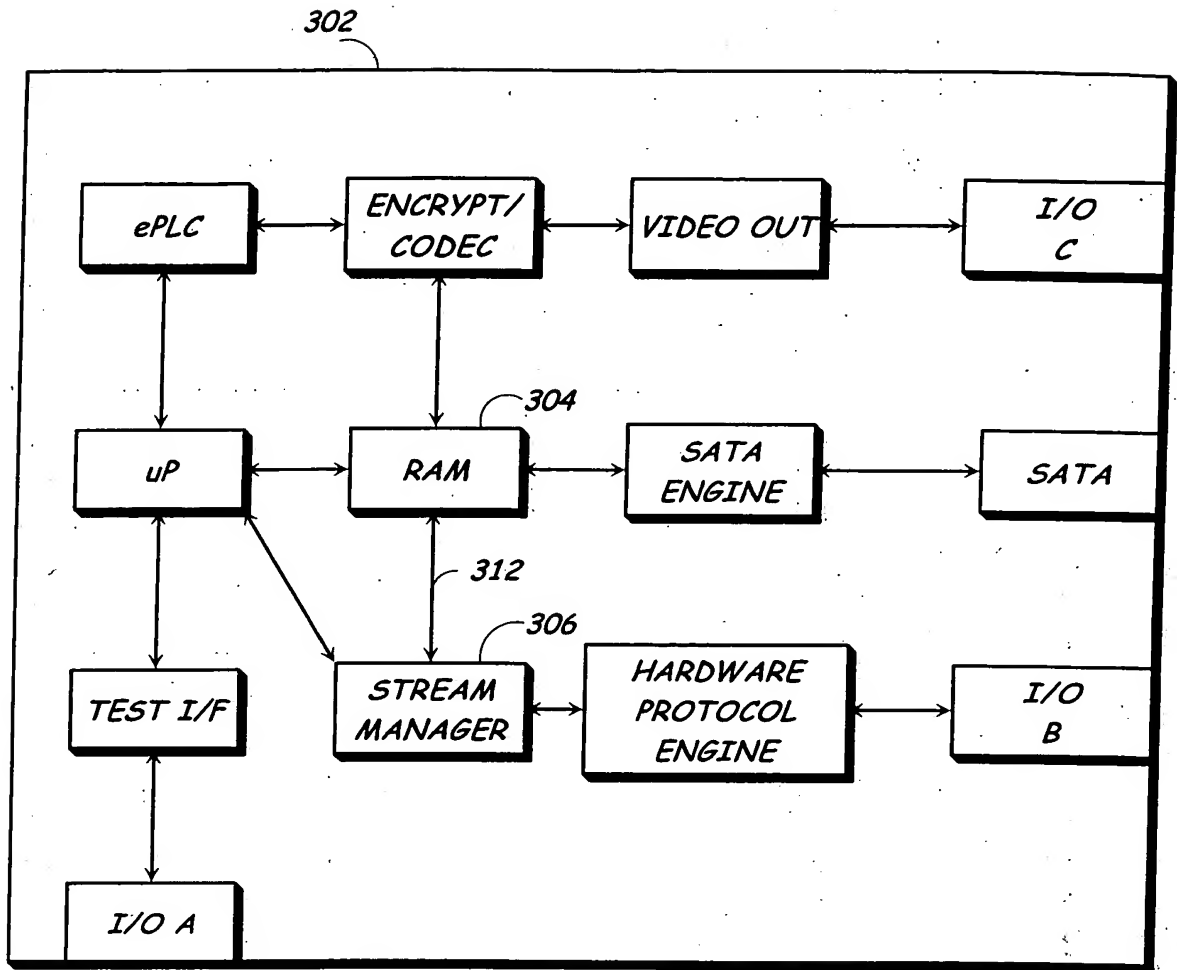


FIG. 4

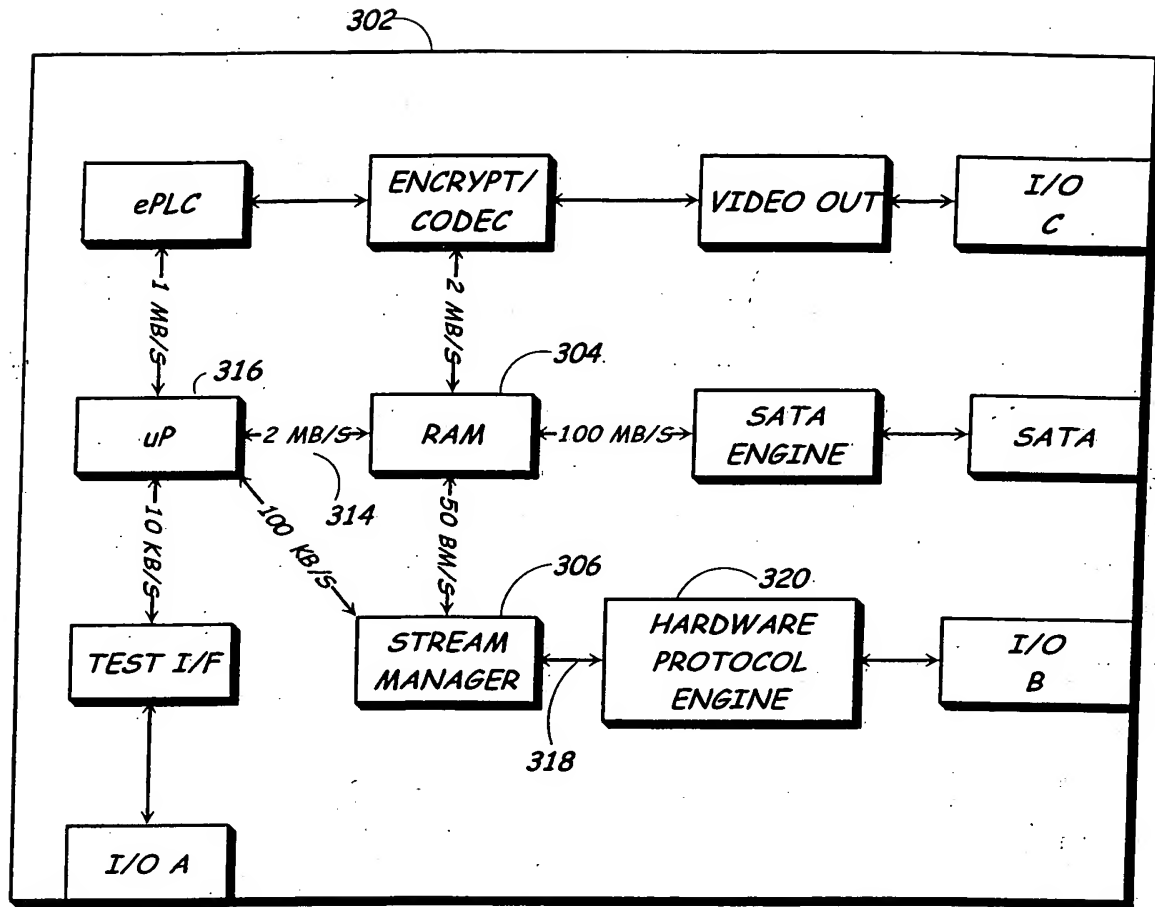


FIG. 5

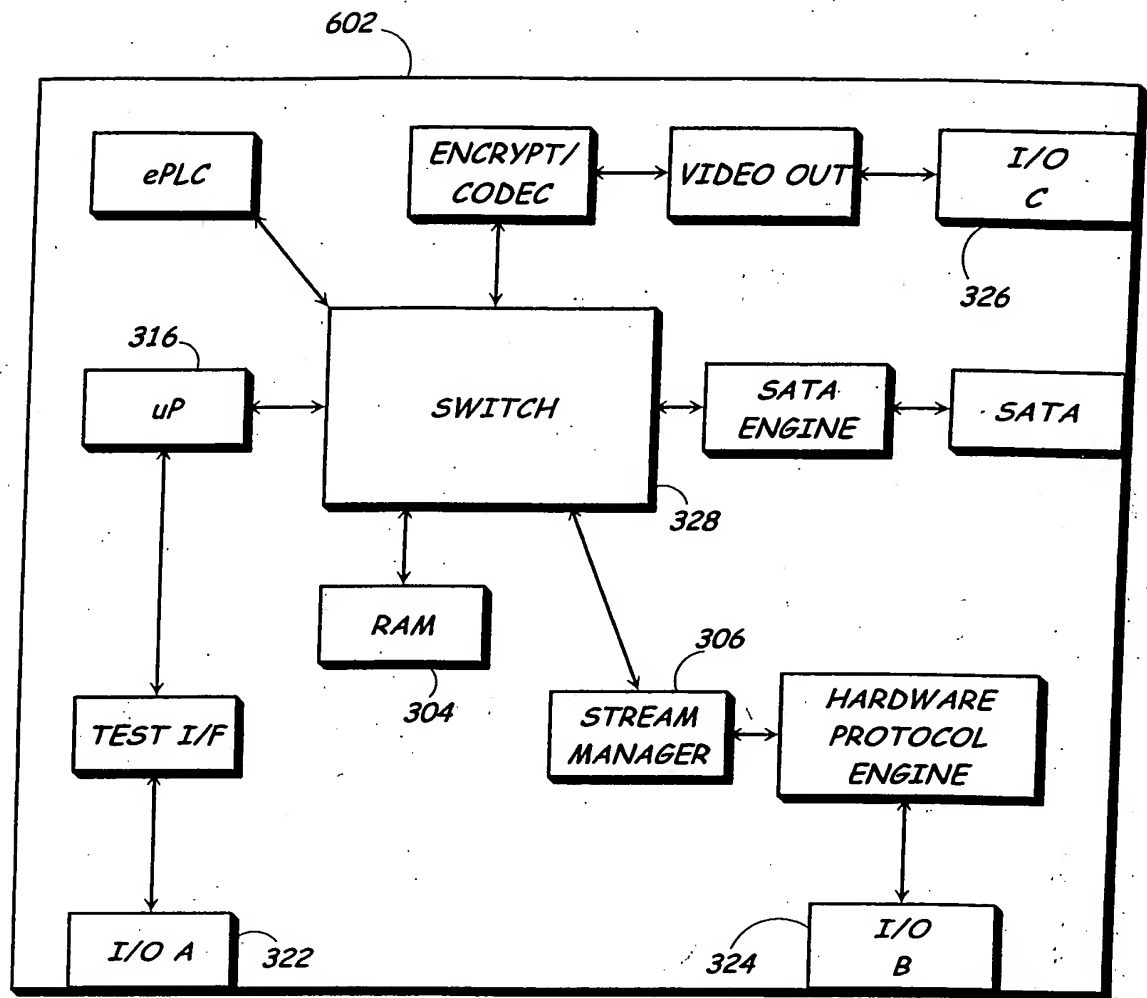


FIG. 6

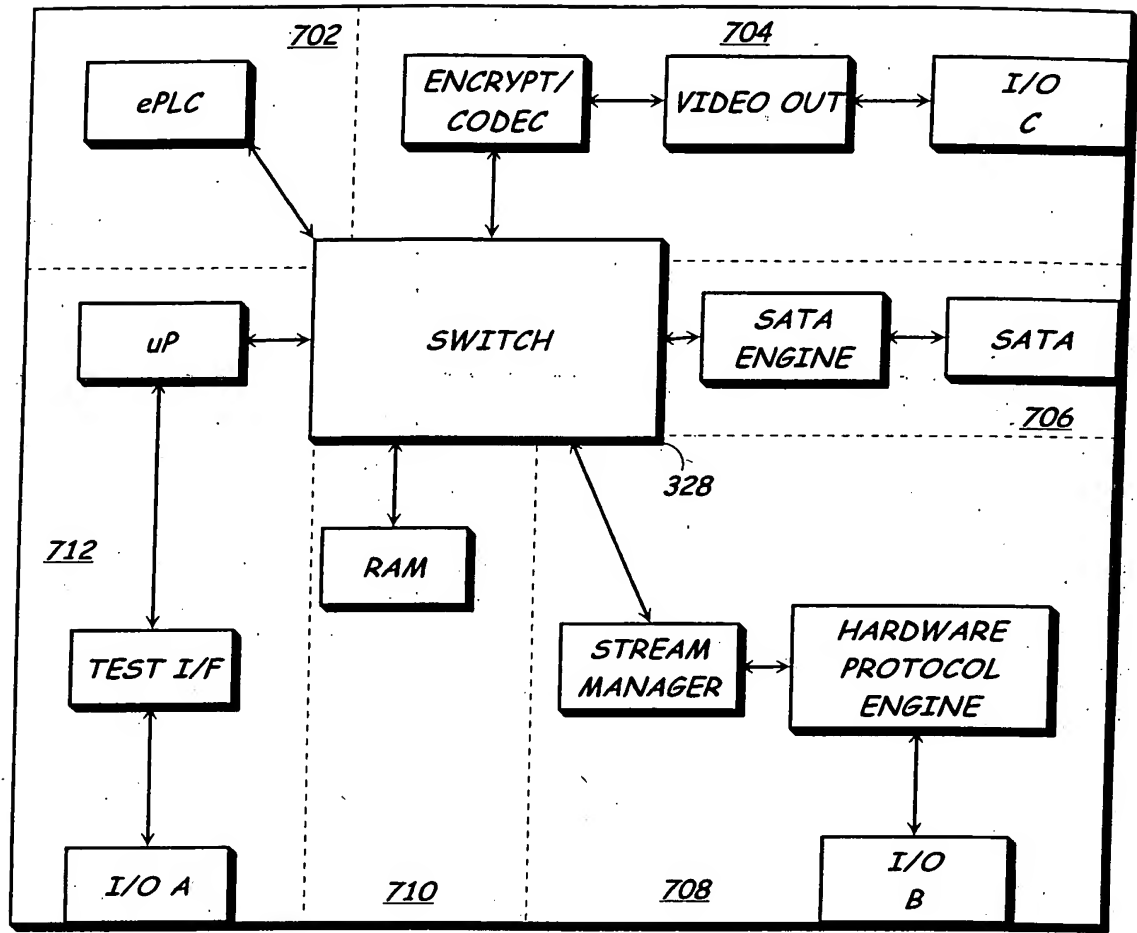


FIG. 7

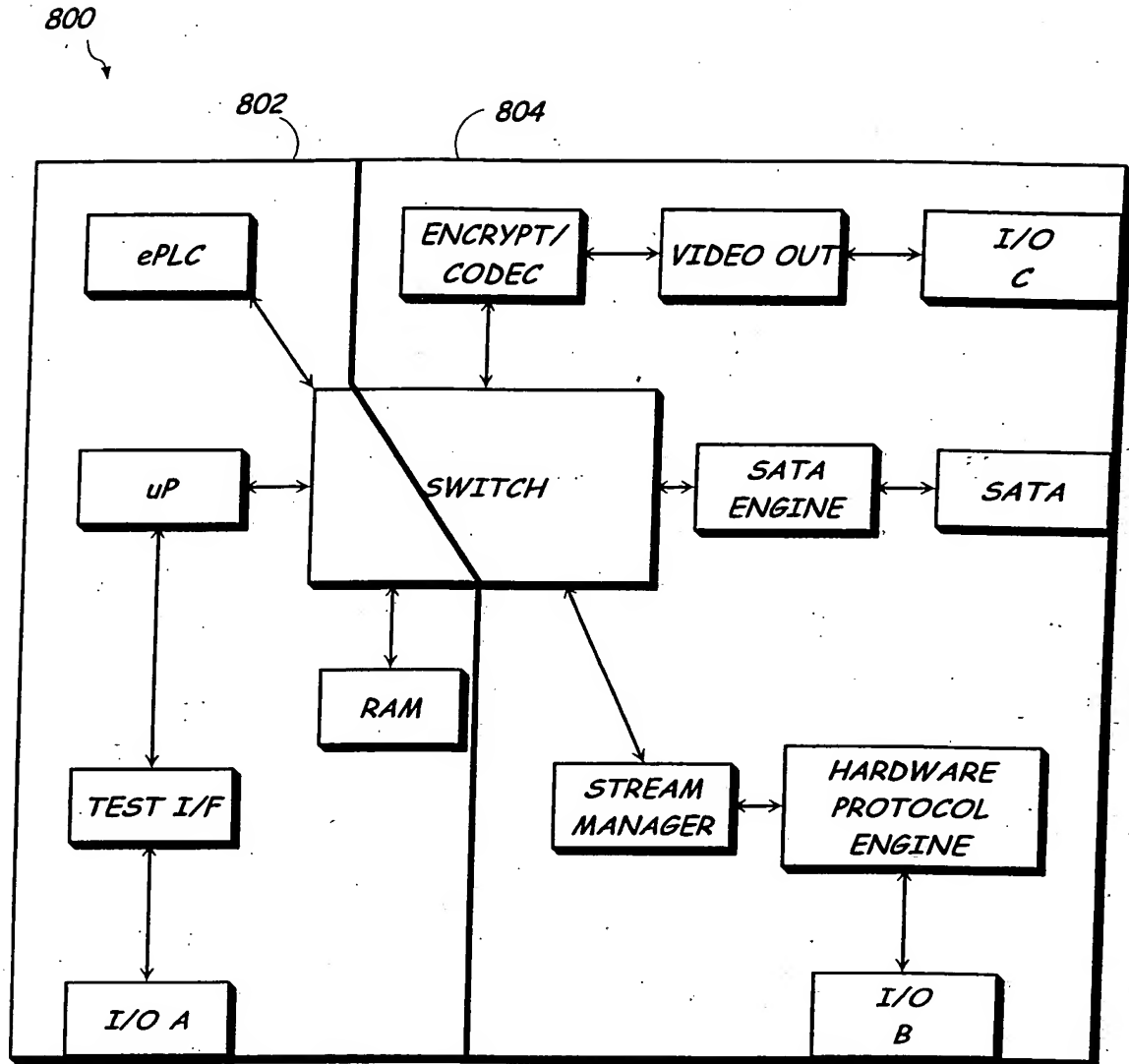


FIG. 8

900

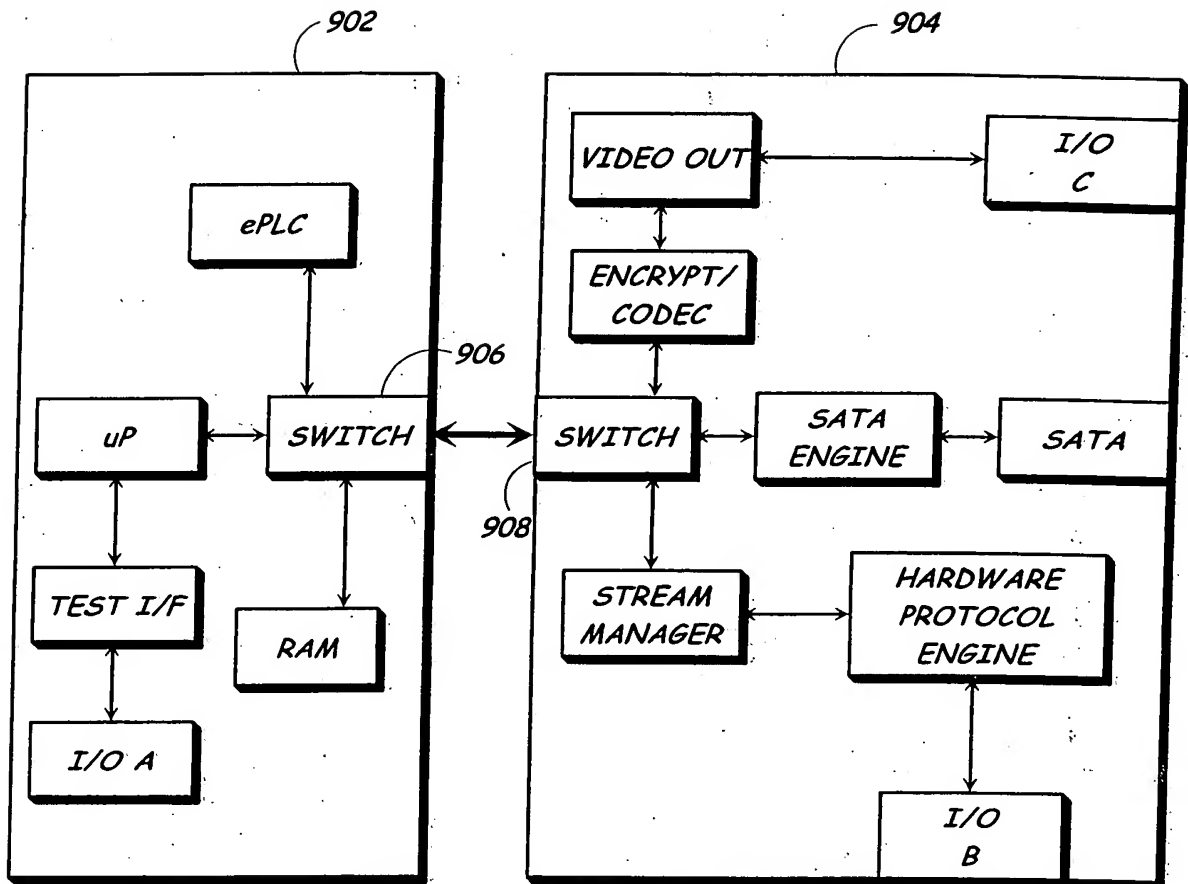


FIG. 9

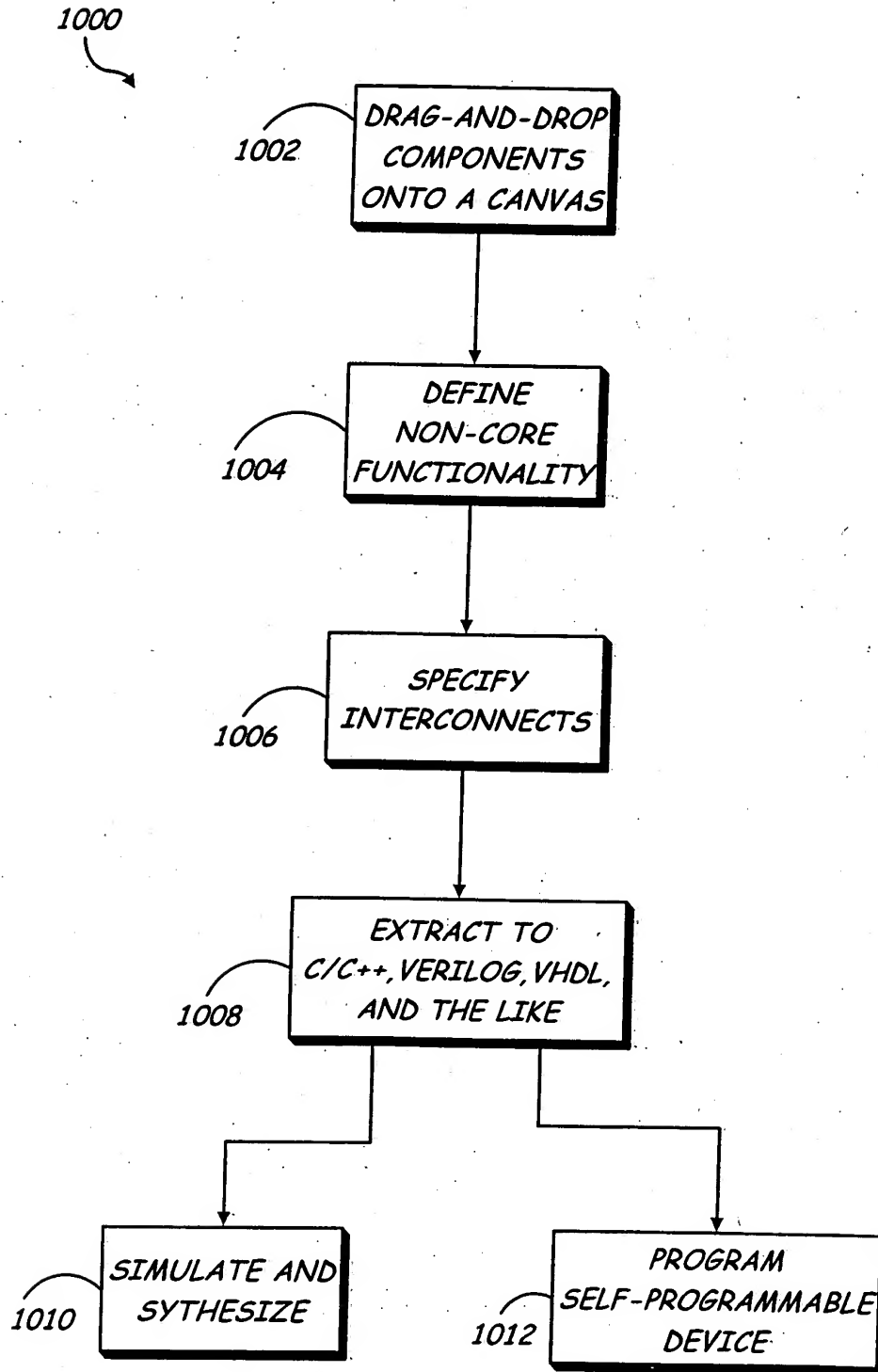


FIG. 10

FOOTNOTES

1100

METHODOLOGY (METASTREAM)

ARCHITECTURAL ENVIRONMENT

CORES, USER FUNCTIONALITY, PARTITIONING, CONNECTIVITY PERFORMANCE, QoS, POWER PROGRAMMABILITY, AND THE LIKE

EXTRACTION PROCESS

1120

RUNTIME
SOFTWARE
INSTANCE(S)

1114

"SILICON" EXTRACTION

1112

1110

CuP MODEL

HARD/SOFT CORES

CUSTOM

1104

TIMING CONSTRAINTS

1102

SILICON SYNTHESIS

CORES

CUSTOM

CuP

ePLC

INTERCONNECT

DEVELOPMENT PROCESS

FIG. 11